Features

- SRAM based FPGA Dedicated to Space Use
- SEE Hardened Cells (configuration RAM, FreeRAM, DFF, JTAG, I/O buffers) Remove the need for Triple Modular Redundancy (TMR)
- Produced on Rad Hard 0.35µm CMOS Process
- Functionally and Pin Compatible with the Atmel Commercial and Military AT40K Series
- High Performance
  - 46K Available ASIC gates (50% typ. routable)
  - 60 MHz Internal Performance
  - 20 MHz System Performance
  - 30 MHz Array Multipliers
  - 18 ns FreeRAM™ access time
  - Internal Tri-state Capability in Each Cell
- FreeRAM
  - 18432 Bits of Distributed SRAM Independent of Logic Cells
  - Flexible, Single/Dual Port, Synchronous/Asynchronous 32x4 RAM blocks
- 8 Global Clocks and 4 Additional Dedicated PCI Clocks
  - Fast, Low Skew Clock Distribution
  - Programmable Rising/Falling Edge Transitions
  - Distributed Clock Shutdown Capability for Low Power Management
- Global Reset Option
- 384 PCI Compliant I/Os
  - Programmable Output Drive
  - Fast, Flexible Array Access Facilitates Pin Locking
- Package Options
  - MQFPF160
  - MQFPF256
- Design Software (System Designer)
  - Combination of Atmel internally developed tools, and industry standard design tools
  - Fast and Efficient Synthesis
  - Efficient Integration (Libraries, Interface, Full Back-annotation)
  - Over 75 Automatic Component Generators Create Thousands of Speed and Area Optimized Logic and RAM Functions
  - Automatic/Interactive Multi-chip Partitioning
- Supply Voltage 3.3V
- AT40KFL040 is a 5V Tolerant Version
- No Single Event Latch-up below a LET Threshold of 70 MeV/mg/cm2
- Tested up to a Total Dose of 300 krads (Si) according to MIL STD 883 Method 1019
- Quality Grades
  - QML -Q and -V with SMD 5962-03250
  - ESCC with 9304/008
- Design Kit (AT40KEL-DK) Including:
  - A Board with the RH FPGA (MQFPF160 or MQFPF256)
  - A configuration memory (AT17 Atmel EEPROM)
  - Design software and documentation
  - ISP cable and software
- Easy Migration to Atmel Gate Arrays for High Volume Production

Note: All features and characteristics described for AT40KEL040 in this document, also apply to the AT40KFL040 unless specified otherwise.

Rad Hard Reprogrammable FPGAs with FreeRAM

AT40KEL040
AT40KFL040

4155I–AERO–06/06

Table 1. AT40KEL040

Device	AT40KEL040
Available ASIC Gates (50% typ. routable)	46K
Rows x Columns	48 x 48
Core Cells	2,304
Registers	3,056
RAM Bits	18,432
I/O (max)	384

Description

The AT40KEL040 is a fully PCI-compliant, SRAM-based FPGA with distributed 18 ns programmable synchronous/asynchronous, dual port/single port SRAM, 8 global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data), automatic component generators, and 46,000 ASIC gates. I/O counts range from 129 to 384 in Aerospace standard packages and support 3.3V.

The AT40KFL040 is a 5V tolerant version.

The AT40KEL040 is designed to quickly implement high performance, large gate count designs through the use of synthesis and schematic-based tools used Windows® / Linux® platform. Atmel's design tools provide easy integration with industry standard tools such as Synplicity, Modelsim and Leonardo Spectrum/Precision Synthesis. See the IDS datasheet for other supported tools.

The AT40KEL040 can be used as a co-processor for high-speed (DSP/processor-based) designs by implementing a variety of compute-intensive, arithmetic functions. These include adaptive finite impulse response (FIR) filters, Fast Fourier Transforms (FFT), convolvers, interpolators and discrete-cosine transforms (DCT) that are required for video compression and decompression, encryption, convolution and other multimedia applications.

Fast, Flexible and Efficient SRAM

The AT40KEL040 FPGA offers a patented distributed 18 ns SRAM capability where the RAM can be used without losing logic resources. Multiple independent, synchronous or asynchronous, dual port or single port RAM functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool.

Fast, Efficient Array and Vector Multipliers

The AT40KEL040's patented 8-sided core cell with direct horizontal, vertical and diagonal cell-to-cell connections implements ultra fast array multipliers without using any busing resources. The AT40KEL040's Cache Logic capability enables a large number of design coefficients and variables to be implemented in a very small amount of silicon, enabling vast improvement in system speed at much lower cost than conventional FPGAs.

Cache Logic Design

The AT40KEL040 is capable of implementing Cache Logic (Dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40KEL040 can act as a reconfigurable co-processor.

Automatic Component Generators

The AT40KEL040 FPGA family is capable of implementing user-defined, automatically generated, macros in multiple designs; speed and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach and minimizes design risk by reusing already

proven functions. The Automatic Component Generators work seamlessly with industry-standard schematic and synthesis tools to create the fastest, most efficient designs available.

The patented AT40KEL040 series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices offer 46,000 usable ASIC gates, and have 3,056 registers. AT40K series FPGAs utilize a reliable 0.35µm single-poly, 4-metal CMOS process and are 100% factory-tested. Atmel's PC- and workstation-based integrated development system (IDS) is used to create AT40KEL040 series designs. Multiple design entry methods are supported.

The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

AT40KEL040 Configurator

Statistics extracted from configuration bitstreams show that the maximum needed size is 1Mbit.

In order to keep the maximum number of pins assigned to signals, it is recommended to use a serial configuration interface.

This is the reason why Atmel proposes a 1Mbit serial EEPROM for configuring the AT40KEL040, the AT17LV010-10DP which is also a 3.3V bias chip. It is packaged into a 28-pin DIL Flat Pack 400mils wide.

This memory has been tested for total dose under bias and unbiased conditions, exhibiting far better results when unbiased; this is the reason why it is recommended to switch off the memory when it is not in the configuration mode.

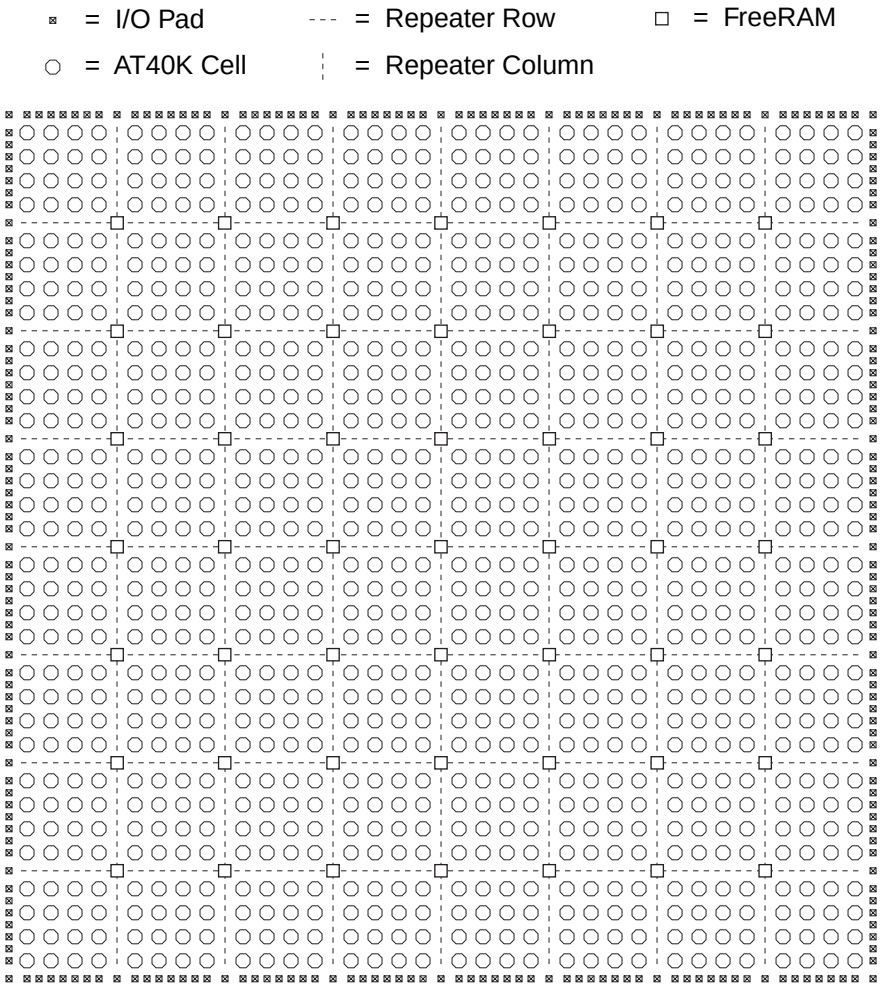
In addition, heavy ions tests have shown that the data stored in the memory cells are not corrupted eventhough errors may be detected while downloading the bitstream; this is the result of the data serialization from the parallel memory plan; therefore, it is recommended to use the FPGA CRC while configuring it, and to resume the configuration when an error is detected.

The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells (Figure 1). The array is continuous from one edge to the other, except for bus repeaters spaced every four cells (Figure 2 on page 5). At the intersection of each repeater row and column is a 32 x 4 RAM block accessible by adjacent buses. The RAM can be configured as either a single-ported or dual-ported RAM[1], with either synchronous or asynchronous operation.

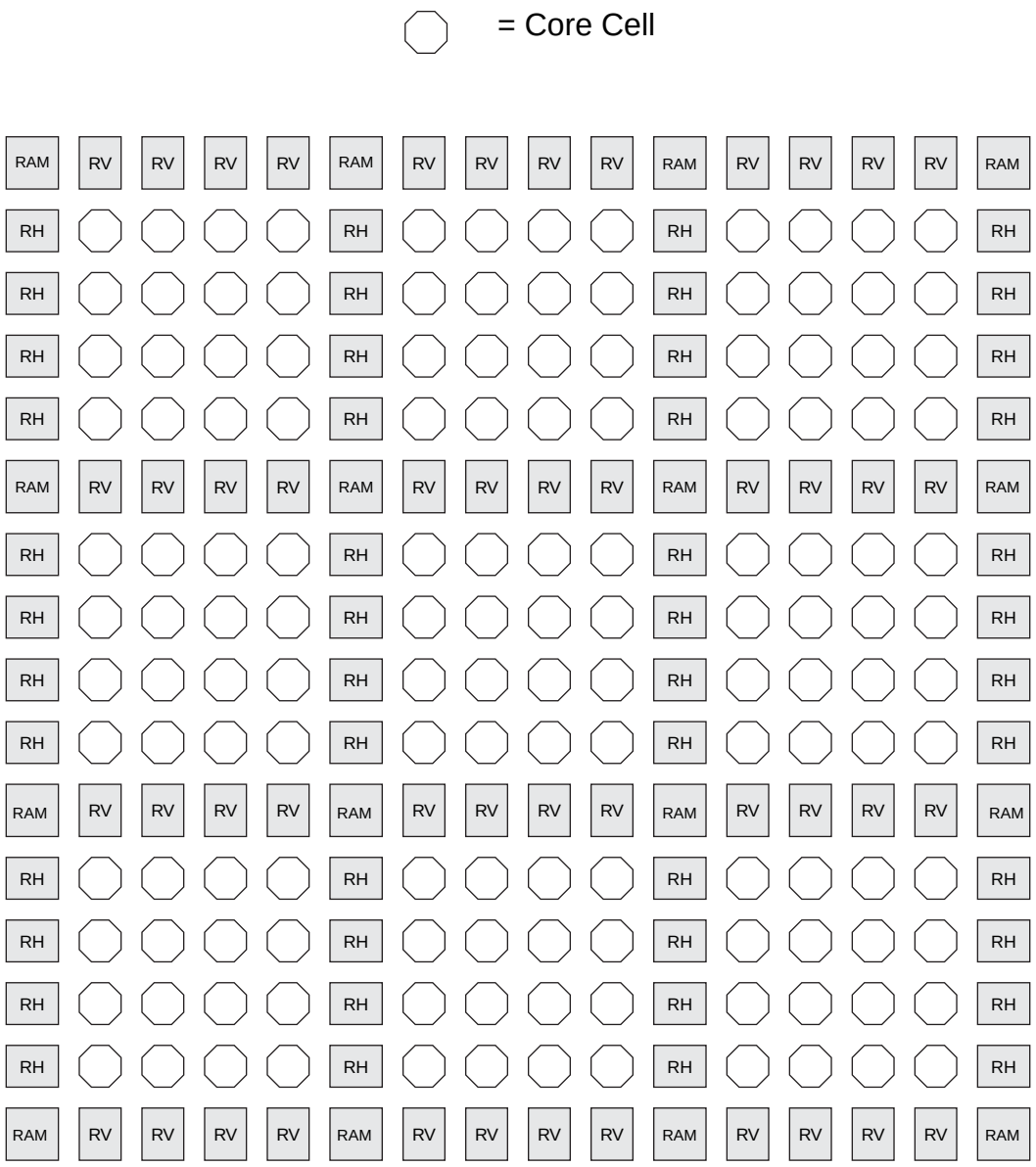
Note: 1. The right-most column can only be used as single-port RAM.

Figure 1. Symmetrical Array Surrounded by I/O



Note: AT40K has registered I/Os. Group enable every sector for tri-states on obuf's.

Figure 2. Floorplan (Representative Portion)[1]



Note: 1. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. This is done automatically using the integrated development system (IDS) tool.

The Busing Network

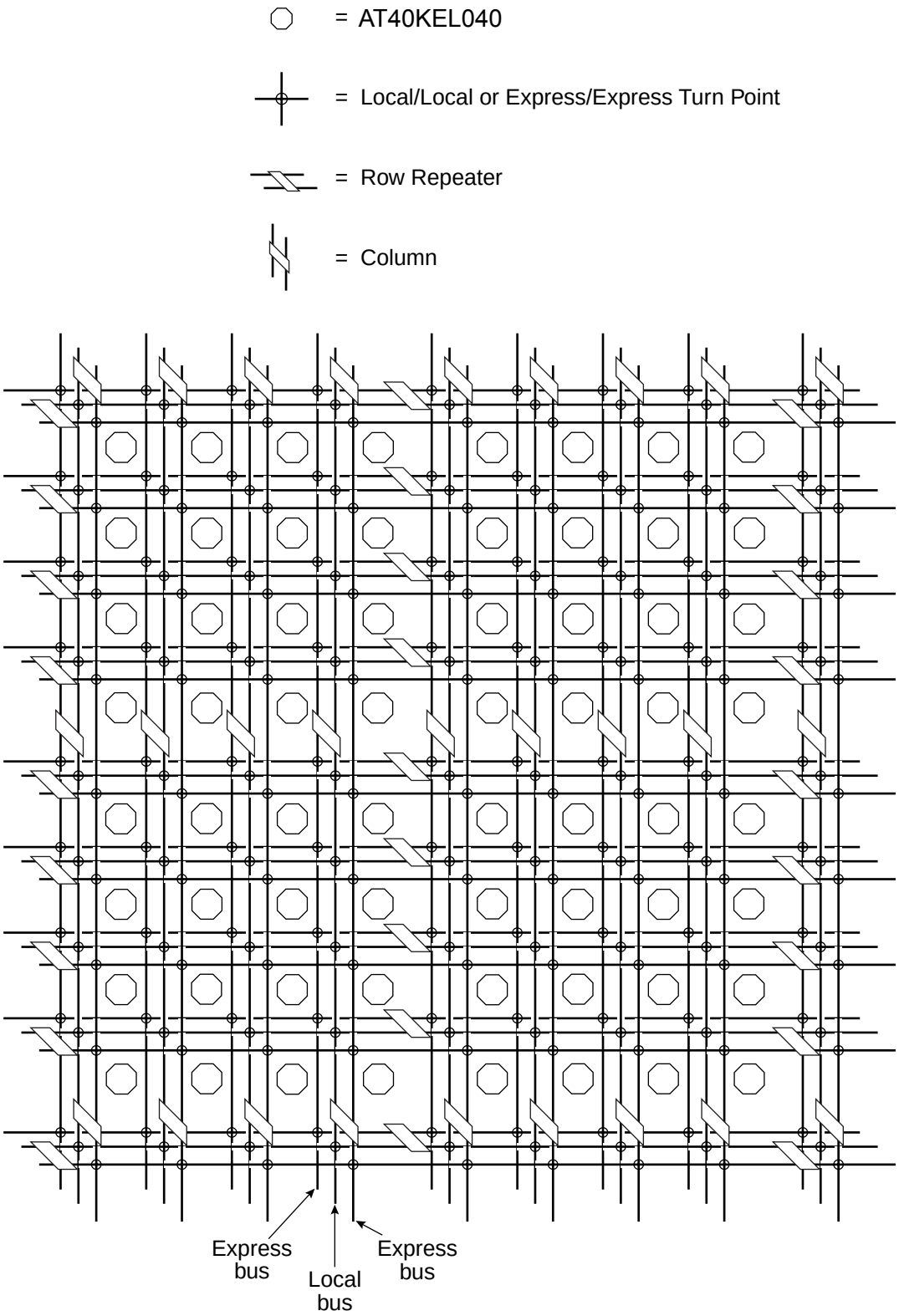
Figure 3 on page 7 depicts one of five identical busing planes. Each plane has three bus resources: a local-bus resource (the middle bus) and two express-bus (both sides) resources. Bus resources are connected via repeaters. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. Each local-bus segment spans four cells and connects to consecutive repeaters. Each express-bus segment spans eight cells and “leapfrogs” or bypasses a repeater. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Although not shown, a local bus can bypass a repeater via a programmable pass gate allowing long on-chip tri-state buses to be created. Local/Local turns are implemented through pass gates in the cell-bus interface (see following page). Express/Express turns are implemented through separate pass gates distributed throughout the array.

Some of the bus resource on the AT40KEL040 is used as a dual-function resource. Table 2 shows which buses are used in a dual-function mode and which bus plane is used. The AT40KEL040 software tools are designed to accommodate dual-function buses in an efficient manner.

Table 2. Dual-function Buses

Function	Type	Plane(s)	Direction	Comments
Cell Output Enable	Local	5	Horizontal and Vertical	
RAM Output Enable	Express	2	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Write Enable	Express	1	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Address	Express	1 - 5	Vertical	Buses full length at array edge Buses in second column to left of RAM block
RAM Data In	Local	1	Horizontal	
RAM Data Out	Local	2	Horizontal	
Clocking	Express	4	Vertical	Bus half length at array edge
Set/Reset	Express	5	Vertical	Bus half length at array edge

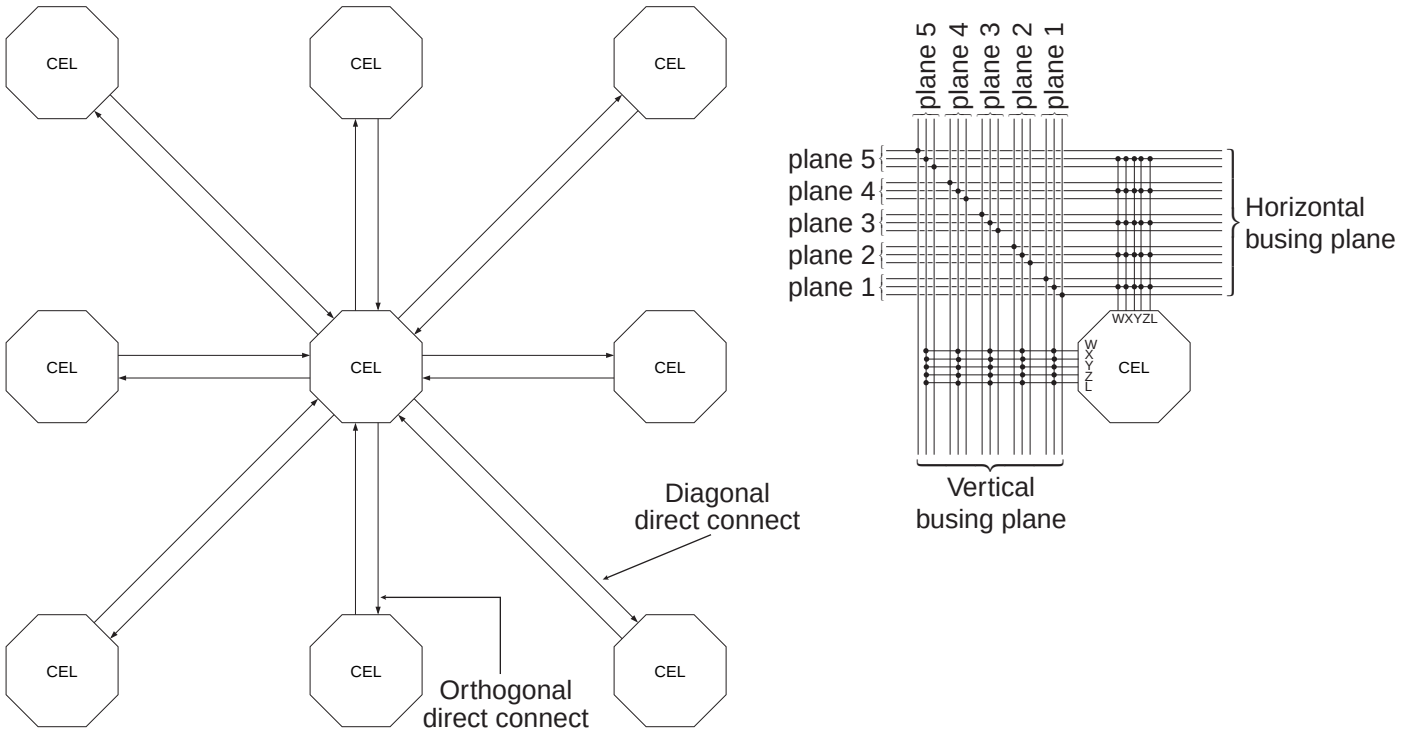
Figure 3. Busing Plane (One of Five)



Cell Connections

Figure 4(a) depicts direct connections between a cell and its eight nearest neighbors. Figure 4(b) shows the connections between a cell and five horizontal local buses (1 per busing plane) and five vertical local buses (1 per busing plane).

Figure 4. Cell Connections



(a) Cell-to-cell Connections

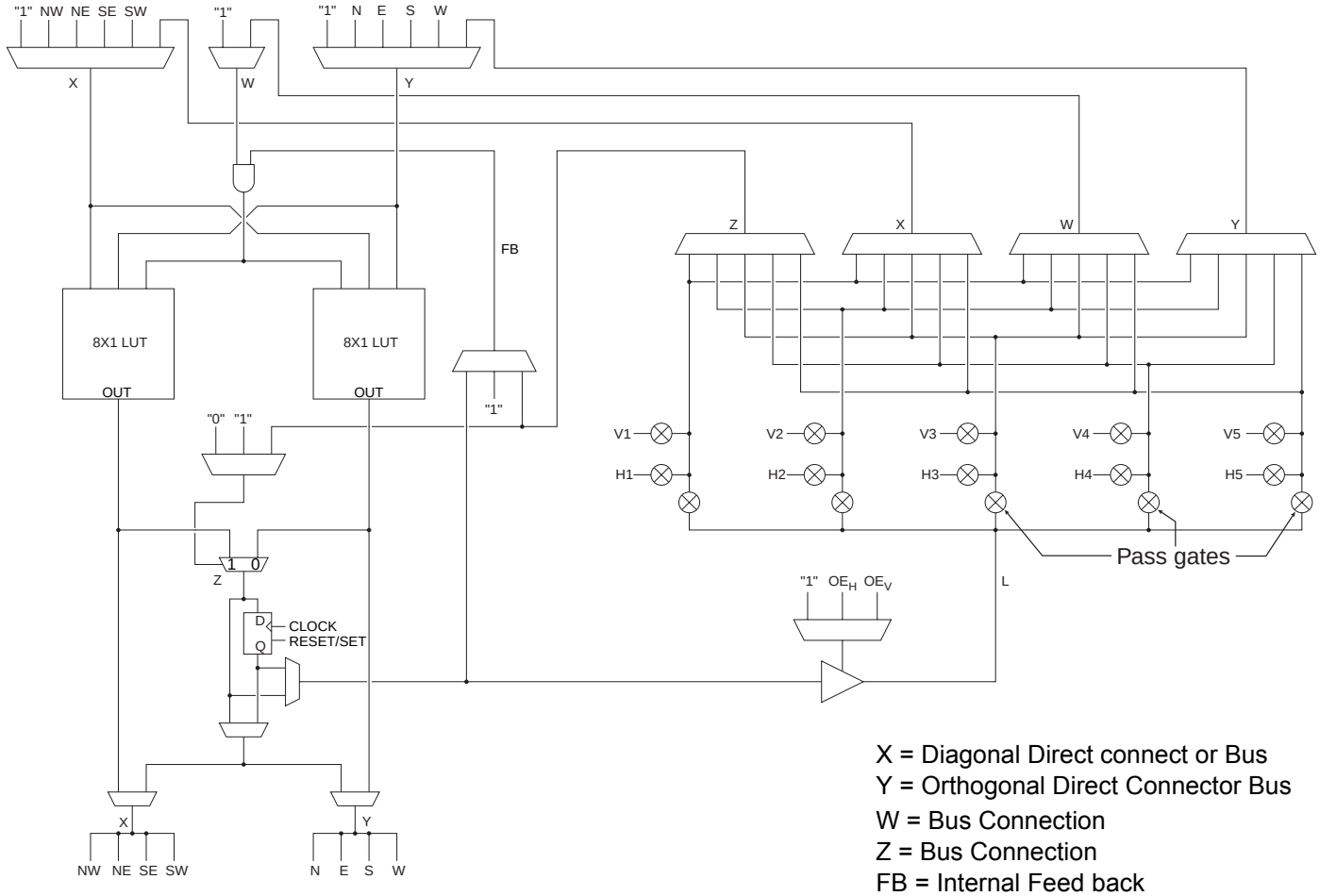
(b) Cell-to-bus Connections

The Cell

Figure 5 depicts the AT40KEL040 cell. Configuration bits for separate muxes and pass gates are independent. All permutations of programmable muxes and pass gates are legal. V_n (V_1 - V_5) is connected to the vertical local bus in plane n. H_n (H_1 - H_5) is connected to the horizontal local bus in plane n. A local/local turn in plane n is achieved by turning on the two pass gates connected to V_n and H_n. Pass gates are opened to let signals into the cell from a local bus or to drive a signal out onto a local bus. Signals coming into the logic cell on one local bus plane can be switched onto another plane by opening two of the pass gates. This allows bus signals to switch planes to achieve greater routability. Up to five simultaneous local/local turns are possible.

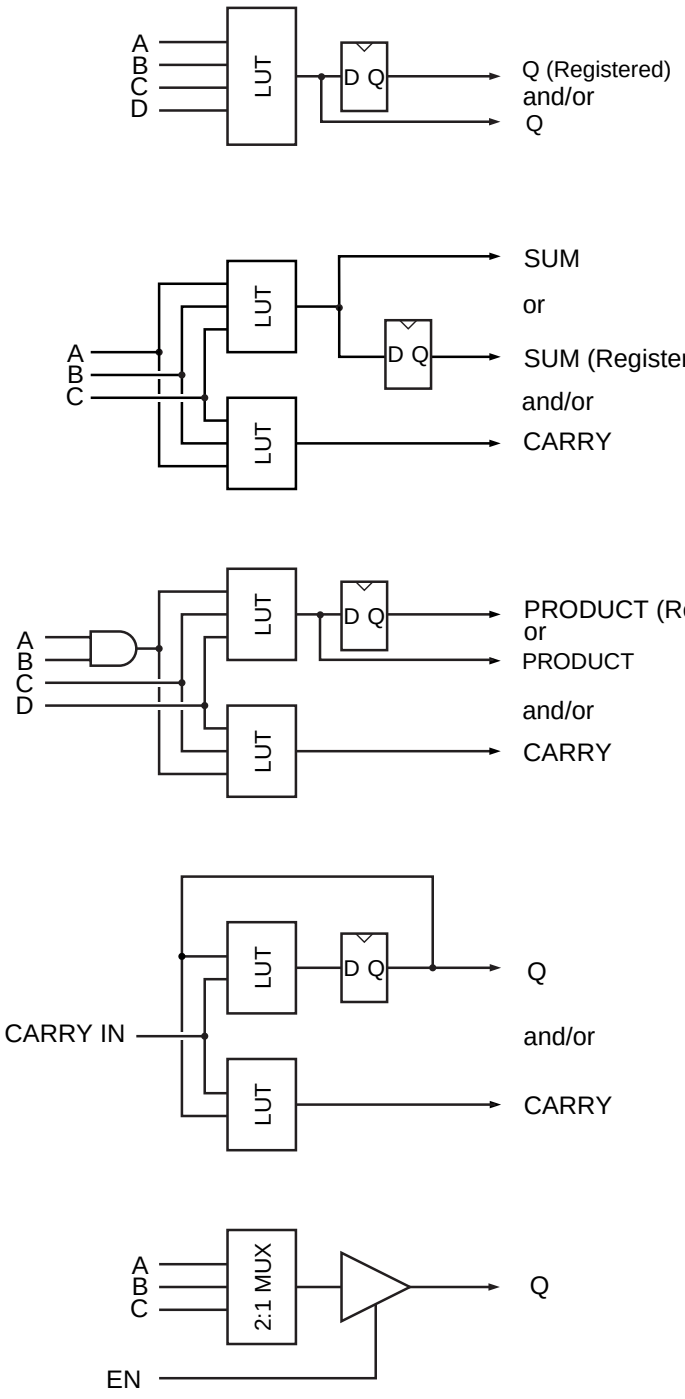
The AT40KEL040 FPGA core cell is a highly configurable logic block based around two 3-input LUTs (8 x 1 ROM), which can be combined to produce one 4-input LUT. This means that any core cell can implement two functions of 3 inputs or one function of 4 inputs. There is a Set/Reset D flip-flop in every cell, the output of which may be tri-stated and fed back internally within the core cell. There is also a 2-to-1 multiplexer in every cell, and an upstream AND gate in the “front end” of the cell. This AND gate is an important feature in the implementation of efficient array multipliers.

Figure 5. The Cell



With this functionality in each core cell, the core cell can be configured in several “modes”. The core cell flexibility makes the AT40KEL040 architecture well suited to most digital design application areas (see Figure 6).

Figure 6. Some Single Cell Modes



Synthesis Mode. This mode is particularly important for the use of VHDL design. VHDL Synthesis tools generally will produce as their output large amounts of random logic functions. Having a 4-input LUT structure gives efficient random logic optimization without the delays associated with larger LUT structures. The output of any cell may be registered, tri-stated and/or fed back into a core cell.

Arithmetic Mode is frequently used in many designs. As can be seen in the figure, the AT40KEL040 core cell can implement a 1-bit full adder (2-input adder with both Carry In and Carry Out) in one core cell. Note that the sum output in this diagram is registered. This output could then be tri-stated and/or fed back into the cell.

DSP/Multiplier Mode. This mode is used to efficiently implement array multipliers. An array multiplier is an array of bitwise multipliers, each implemented as a full adder with an upstream AND gate. Using this AND gate and the diagonal interconnects between cells, the array multiplier structure fits very well into the AT40K architecture.

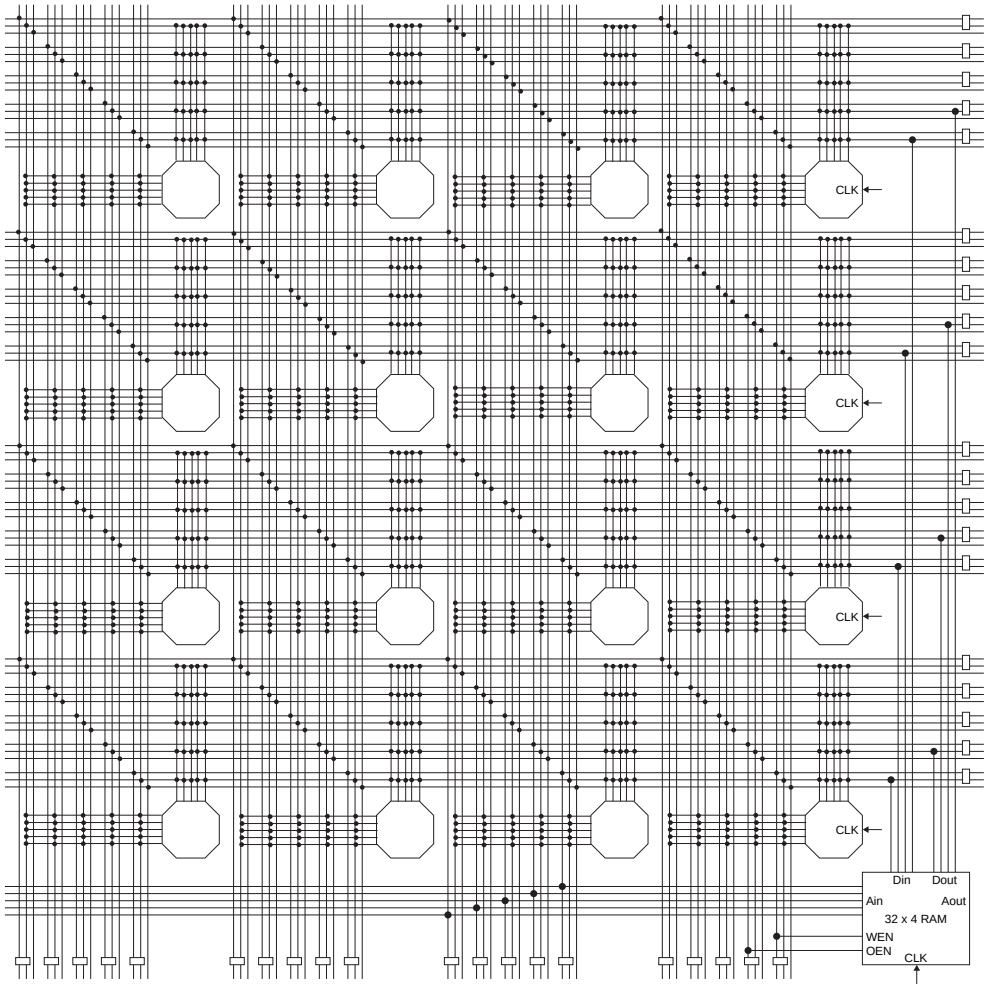
Counter Mode. Counters are fundamental to almost all digital designs. They are the basis of state machines, timing chains and clock dividers. A counter is essentially an increment by one function (i.e., an adder), with the input being an output (or a decode of an output) from the previous stage. A 1-bit counter can be implemented in one core cell. Again, the output can be registered, tri-stated and/or fed back.

Tri-state/Mux Mode. This mode is used in many telecommunications applications, where data needs to be routed through more than one possible path. The output of the core cell is very often tri-statable for many inputs to many outputs data switching.

RAM

32 x 4 dual-ported RAM blocks are dispersed throughout the array as shown in Figure 7. A 4-bit Input Data Bus connects to four horizontal local buses distributed over four sector rows (plane 1). A 4-bit Output Data Bus connects to four horizontal local buses distributed over four sector rows (plane 2). A 5-bit Input Address Bus connects to five vertical express buses in same column. A 5-bit Output Address Bus connects to five vertical express buses in same column. Ain (input address) and Aout (output address) alternate positions in horizontally aligned RAM blocks. For the left-most RAM blocks, Aout is on the left and Ain is on the right. For the right-most RAM blocks, Ain is on the left and Aout is tied off, thus it can only be configured as a single port. For single-ported RAM, Ain is the READ/WRITE address port and Din is the (bi-directional) data port. Right-most RAM blocks can be used only for single-ported memories. WEN and OEN connect to the vertical express buses in the same column.

Figure 7. RAM Connections (One Ram Block)



Reading and writing of the 18 ns 32 x 4 dual-port FreeRAM are independent of each other. Reading the 32 x 4 dual-port RAM is completely asynchronous. Latches are transparent; when Load is logic 1, data flows through; when Load is logic 0, data is latched. These latches are used to synchronize Write Adress, Write Enable Not, and Din signals for a synchronous RAM. Each bit in the 32 x 4 dual-port RAM is also a transparent latch. The front-end latch and the memory latch together form an edge-triggered flip flop. When a nibble (bit = 7) is (Write) addressed and LOAD is logic 1 and $\overline{WE}$ is logic 0,

data flows through the bit. When a nibble is not (Write) addressed or LOAD is logic 0 or WE is logic 1, data is latched in the nibble. The two CLOCK muxes are controlled together; they both select CLOCK (for a synchronous RAM) or they both select “1” (for an asynchronous RAM). CLOCK is obtained from the clock for the sector-column immediately to the left and immediately above the RAM block. Writing any value to the RAM clear byte during configuration clears the RAM (see the “*AT40K/40KAL Configuration Series”* application note at www.atmel.com).

Figure 8. RAM Logic

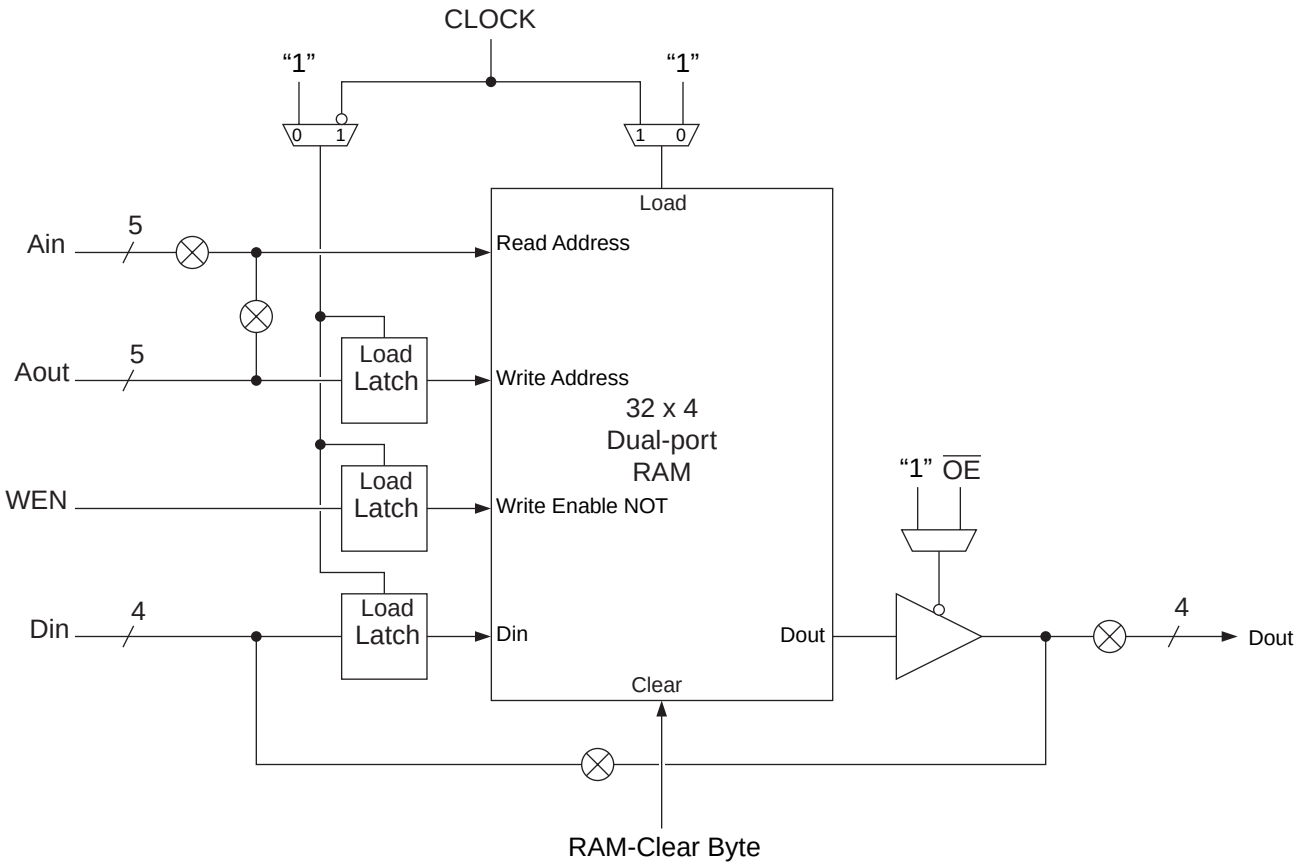
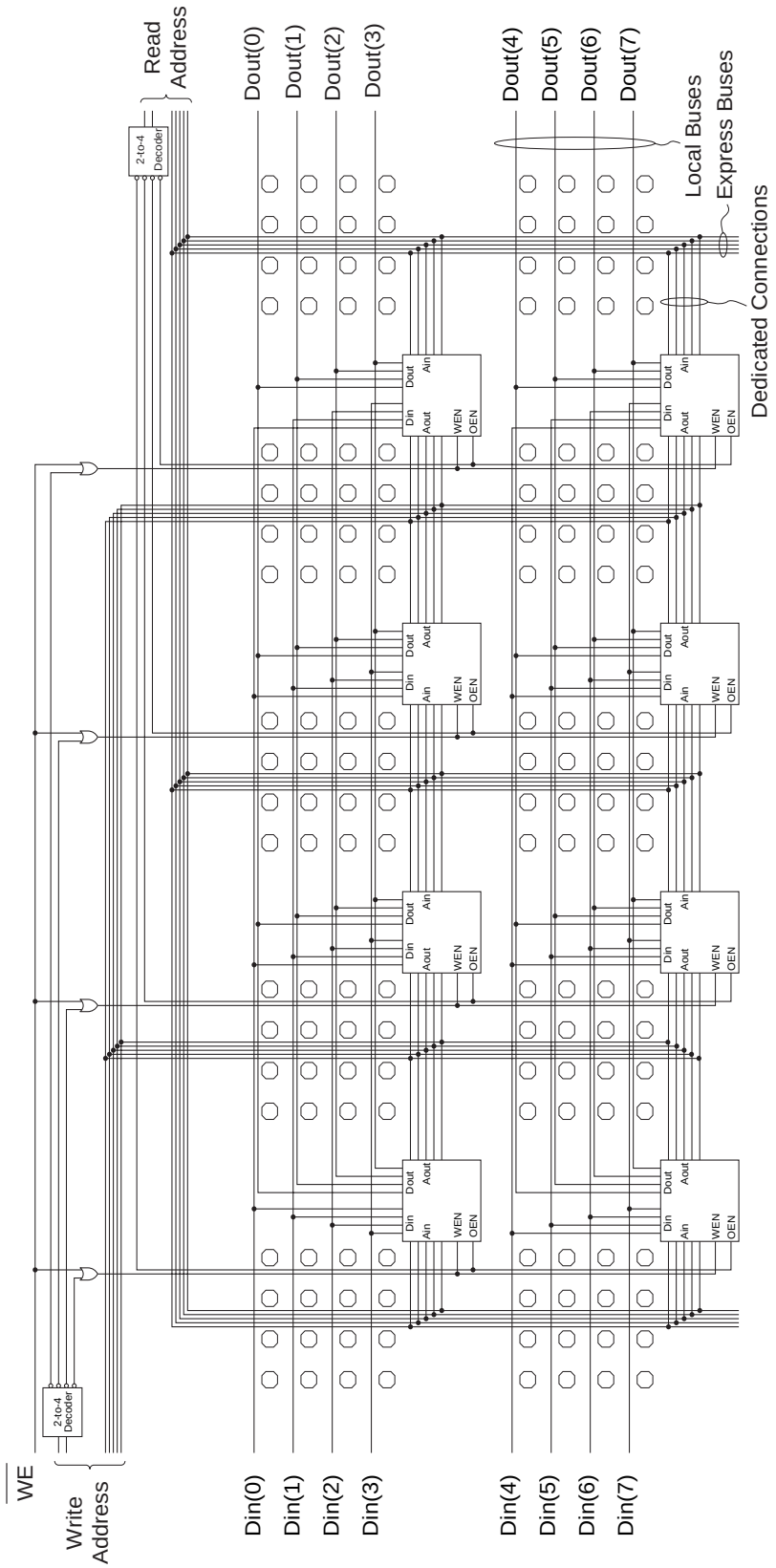


Figure 9 on page 13 shows an example of a RAM macro constructed using AT40KEL040’s FreeRAM cells. The macro shown is a 128 x 8 dual-ported asynchronous RAM. Note the very small amount of external logic required to complete the address decoding for the macro. Most of the logic cells (core cells) in the sectors occupied by the RAM will be unused: they can be used for other logic in the design. This logic can be automatically generated using the macro generators.

Figure 9. RAM Example: 128 x 8 Dual-ported RAM (Asynchronous)



Clocking Scheme

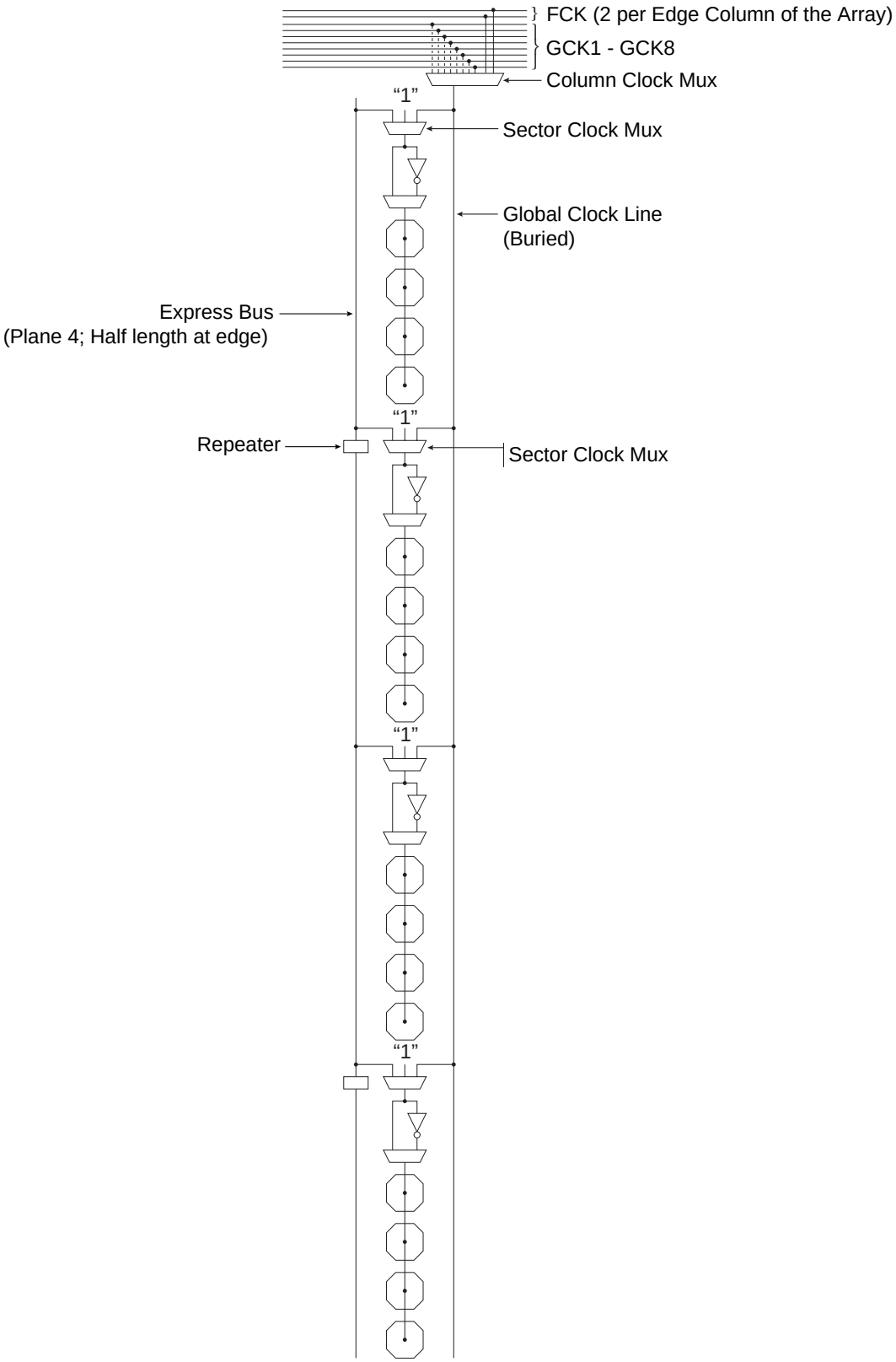
There are eight Global Clock buses (GCK1 - GCK8) on the AT40KEL040 FPGA. Each of the eight dedicated Global Clock buses is connected to one of the dual-use Global Clock pins. Any clocks used in the design should use global clocks where possible: this can be done by using Assign Pin Locks to lock the clocks to the Global Clock locations. In addition to the eight Global Clocks, there are four Fast Clocks (FCK1 - FCK4), two per edge column of the array for PCI specification. Even the derived clocks can be routed through the Global network. Access points are provided in the corners of the array to route the derived clocks into the global clock network. The IDS software tools handle derived clocks to global clock connections automatically if used.

Each column of an array has a “Column Clock mux” and a “Sector Clock mux”. The Column Clock mux is at the top of every column of an array and the Sector Clock mux is at every four cells. The Column Clock mux is selected from one of the eight Global Clock buses. The clock provided to each sector column of four cells is inverted, non-inverted or tied off to “0”, using the Sector Clock mux to minimize the power consumption in a sector that has no clocks. The clock can either come from the Column Clock or from the Plane 4 express bus (see Figure 10 on page 15). The extreme-left Column Clock mux has two additional inputs, FCK1 and FCK2, to provide fast clocking to left-side I/Os. The extreme-right Column Clock mux has two additional inputs as well, FCK3 and FCK4, to provide fast clocking to right-side I/Os.

The register in each cell is triggered on a rising clock edge by default. Before configuration on power-up, constant “0” is provided to each register’s clock pins. After configuration on power-up, the registers either set or reset, depending on the user’s choice.

The clocking scheme is designed to allow efficient use of multiple clocks with low clock skew, both within a column and across the core cell array.

Figure 10. Clocking (for One Column of Cells)



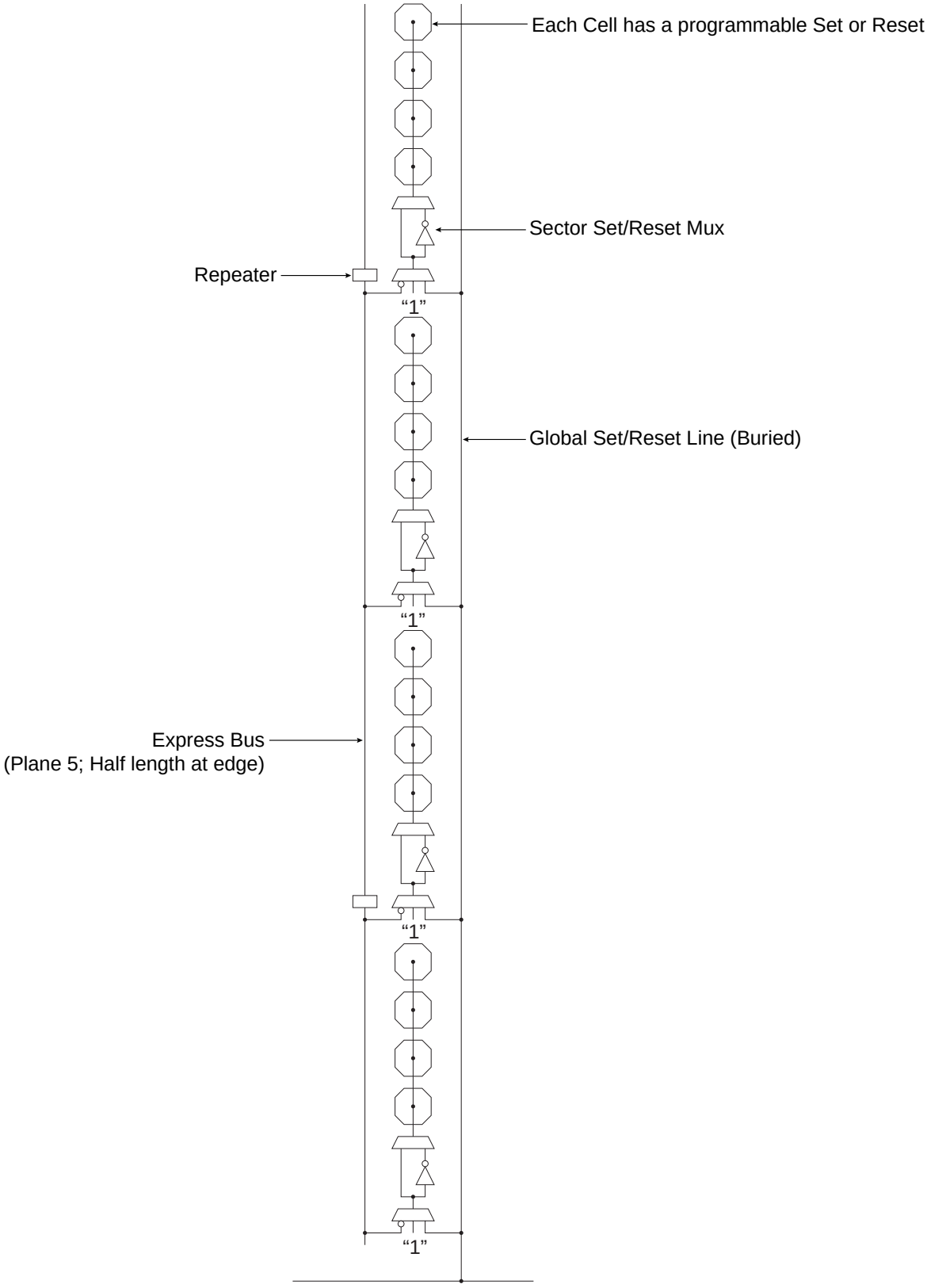
Set/Reset Scheme

The AT40KEL040 family reset scheme is essentially the same as the clock scheme except that there is only one Global Reset. A dedicated Global Set/Reset bus can be driven by any User I/O, except those used for clocking (Global Clocks or Fast Clocks). The automatic placement tool will choose the reset net with the most connections to use the global resources. You can change this by using an RSBUF component in your design to indicate the global reset. Additional resets will use the express bus network.

The Global Set/Reset is distributed to each column of the array. Like Sector Clock mux, there is Sector Set/Reset mux at every four cells. Each sector column of four cells is set/reset by a Plane 5 express bus or Global Set/Reset using the Sector Set/Reset mux (Figure 11 on page 17). The set/reset provided to each sector column of four cells is either inverted or non-inverted using the Sector Reset mux.

The function of the Set/Reset input of a register is determined by a configuration bit in each cell. The Set/Reset input of a register is active low (logic 0) by default. Setting or Resetting of a register is asynchronous. Before configuration on power-up, a logic 1 (a high) is provided by each register (i.e., all registers are set at power-up).

Figure 11. Set/Reset (for One Column of Cells)



I/O Structure

AT40K has registered I/Os and group enable every sector for tri-states on obuf's.

Pad

The I/O pad is the one that connects the I/O to the outside world. Note that not all I/Os have pads: the ones without pads are called Unbonded I/Os. The number of unbonded I/Os varies with the device size and package. These unbonded I/Os are used to perform a variety of bus turns at the edge of the array.

Pull-up/Pull-down

Each pad has a programmable pull-up and pull-down attached to it. This supplies a weak "1" or "0" level to the pad pin. When all other drivers are off, this control will dictate the signal level of the pad pin.

The input stage of each I/O cell has a number of parameters that can be programmed either as properties in schematic entry or in the I/O Pad Attributes editor in IDS.

CMOS

The threshold level is a CMOS-compatible level.

Schmitt

A Schmitt trigger circuit can be enabled on the inputs. The Schmitt trigger is a regenerative comparator circuit that adds 1V hysteresis to the input. This effectively improves the rise and fall times (leading and trailing edges) of the incoming signal and can be useful for filtering out noise.

Delays

The input buffer can be programmed to include four different intrinsic delays as specified in the AC timing characteristics. This feature is useful for meeting data hold requirements for the input signal.

Drive

The output drive capabilities of each I/O are programmable. They can be set to FAST, MEDIUM or SLOW (using IDS tool). The FAST setting has the highest drive capability (16 mA at 3.3V) buffer and the fastest slew rate. MEDIUM produces a medium drive (12 mA at 3.3V) buffer, while SLOW yields a standard (4 mA at 3.3V) buffer.

Tri-State

The output of each I/O can be made tri-state (0, 1 or Z), open source (1 or Z) or open drain (0 or Z) by programming an I/O's Source Selection mux. Of course, the output can be normal (0 or 1), as well.

Source Selection Mux

The Source Selection mux selects the source for the output signal of an I/O. See Figure 12 on page 21.

Primary, Secondary and Corner I/Os

The AT40KEL040 has three kinds of I/Os: Primary I/O, Secondary I/O and a Corner I/O. Every edge cell except corner cells on the AT40KEL040 has access to one Primary I/O and two Secondary I/Os.

Primary I/O

Every logic cell at the edge of the FPGA array has a direct orthogonal connection to and from a Primary I/O cell. The Primary I/O interfaces directly to its adjacent core cell. It also connects into the repeaters on the row immediately above and below the adjacent core cell. In addition, each Primary I/O also connects into the busing network of the three nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Primary I/O can be accessed from any logic cell on three separate rows or columns of the FPGA. See Figures 12a and 13a.

Secondary I/O

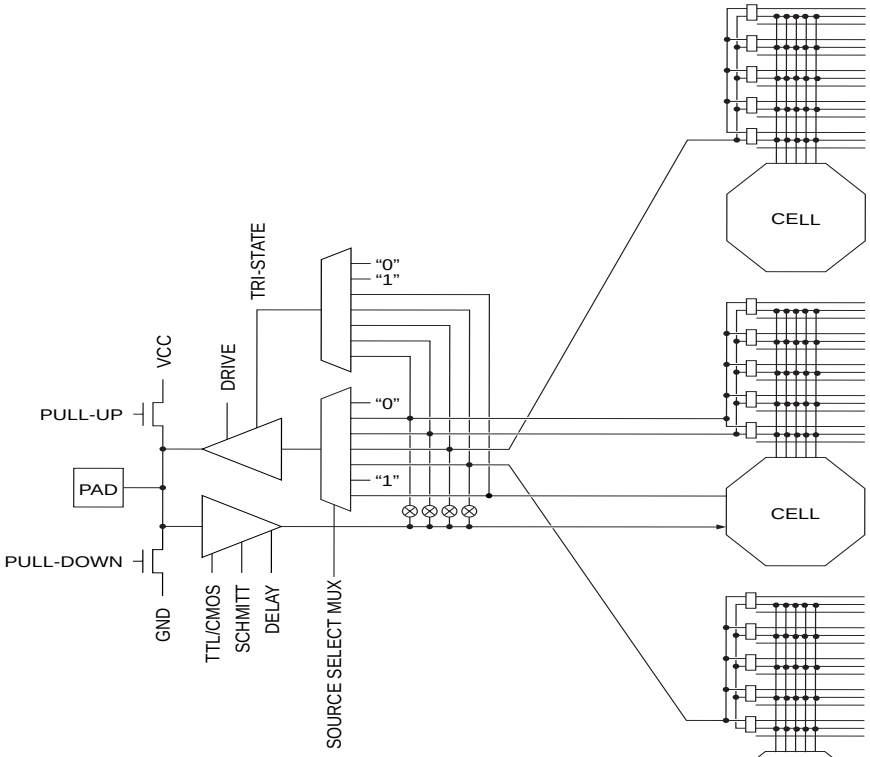
Every logic cell at the edge of the FPGA array has two direct diagonal connections to a Secondary I/O cell. The Secondary I/O is located between core cell locations. This I/O

connects on the diagonal inputs to the cell above and the cell below. It also connects to the repeater of the cell above and below. In addition, each Secondary I/O also connects into the busing network of the two nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Secondary I/O can be accessed from any logic cell on two rows or columns of the FPGA. See Figure 12a and Figure 13b.

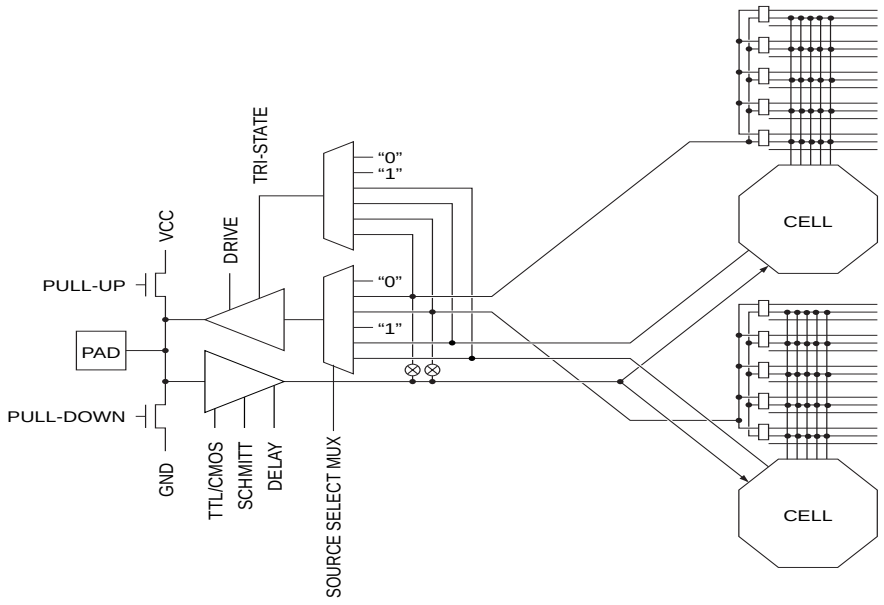
Corner I/O

Logic cells at the corner of the FPGA array have direct-connect access to five separate I/Os: 2 Primary, 2 Secondary and 1 Corner I/O. Corner I/Os are like an extra Secondary I/O at each corner of the array. With the inclusion of Corner I/Os, an AT40KEL040 FPGA with n x n core cells always has 8n I/Os. As the diagram shows, Corner I/Os can be accessed both from the corner logic cell and the horizontal and vertical busing networks running along the edges of the array. This means that many different edge logic cells can access the Corner I/Os. See Figure 14.

Figure 12. South I/O (Mirrored for North I/O)

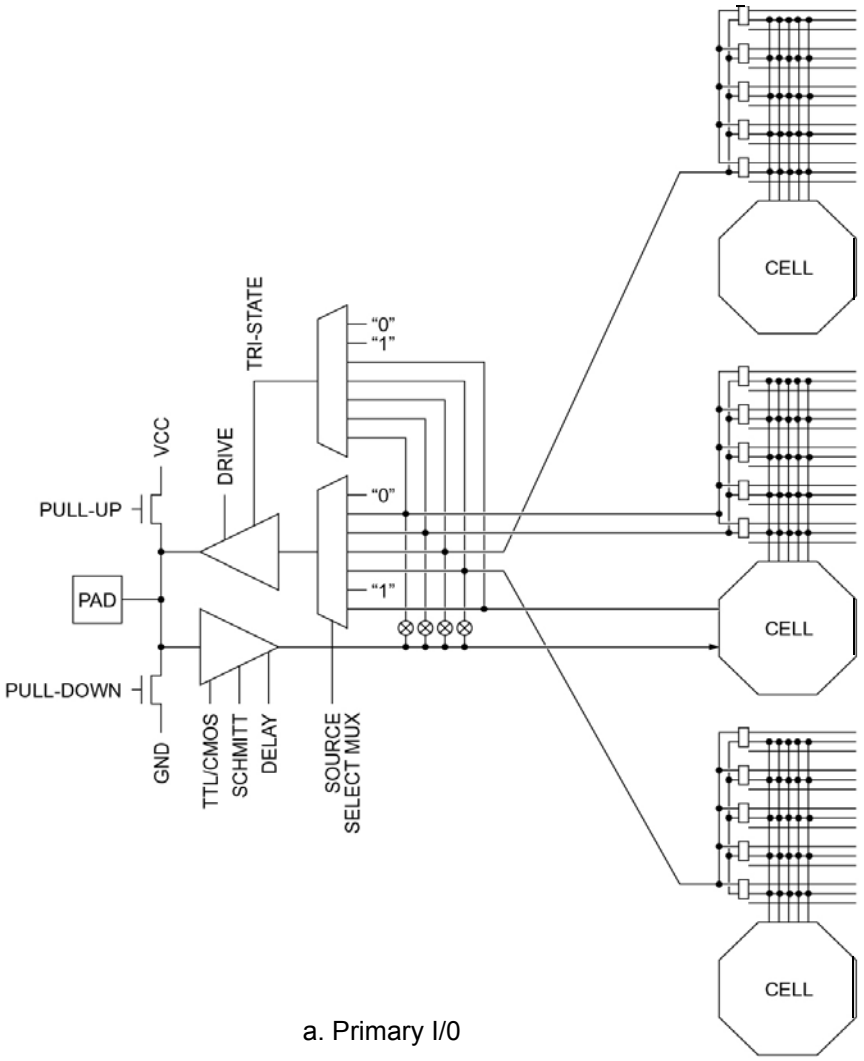


(a) Primary I/O

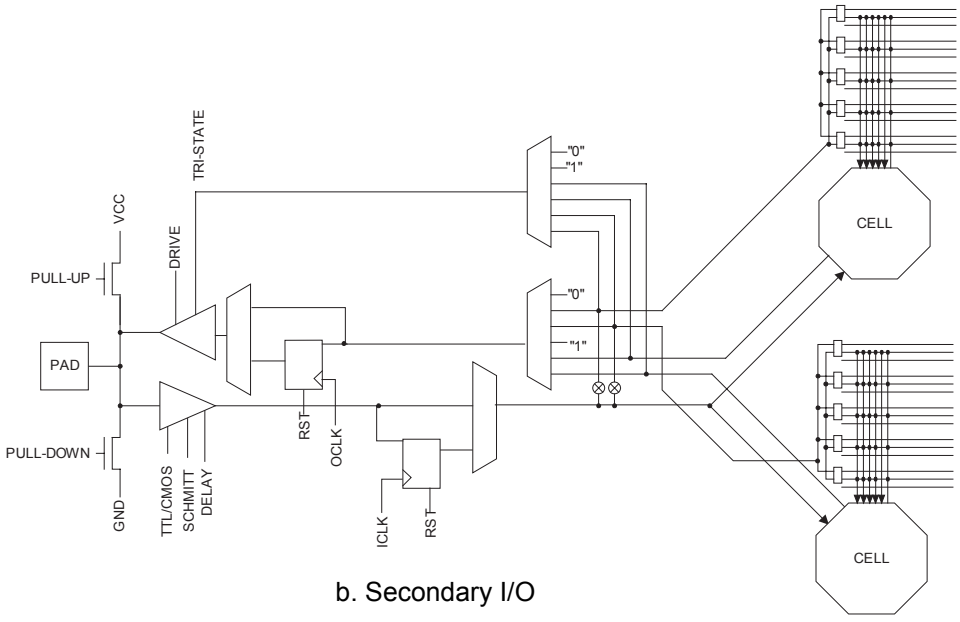


(b) Secondary I/O

Figure 13. West I/O (Mirrored for East I/O)

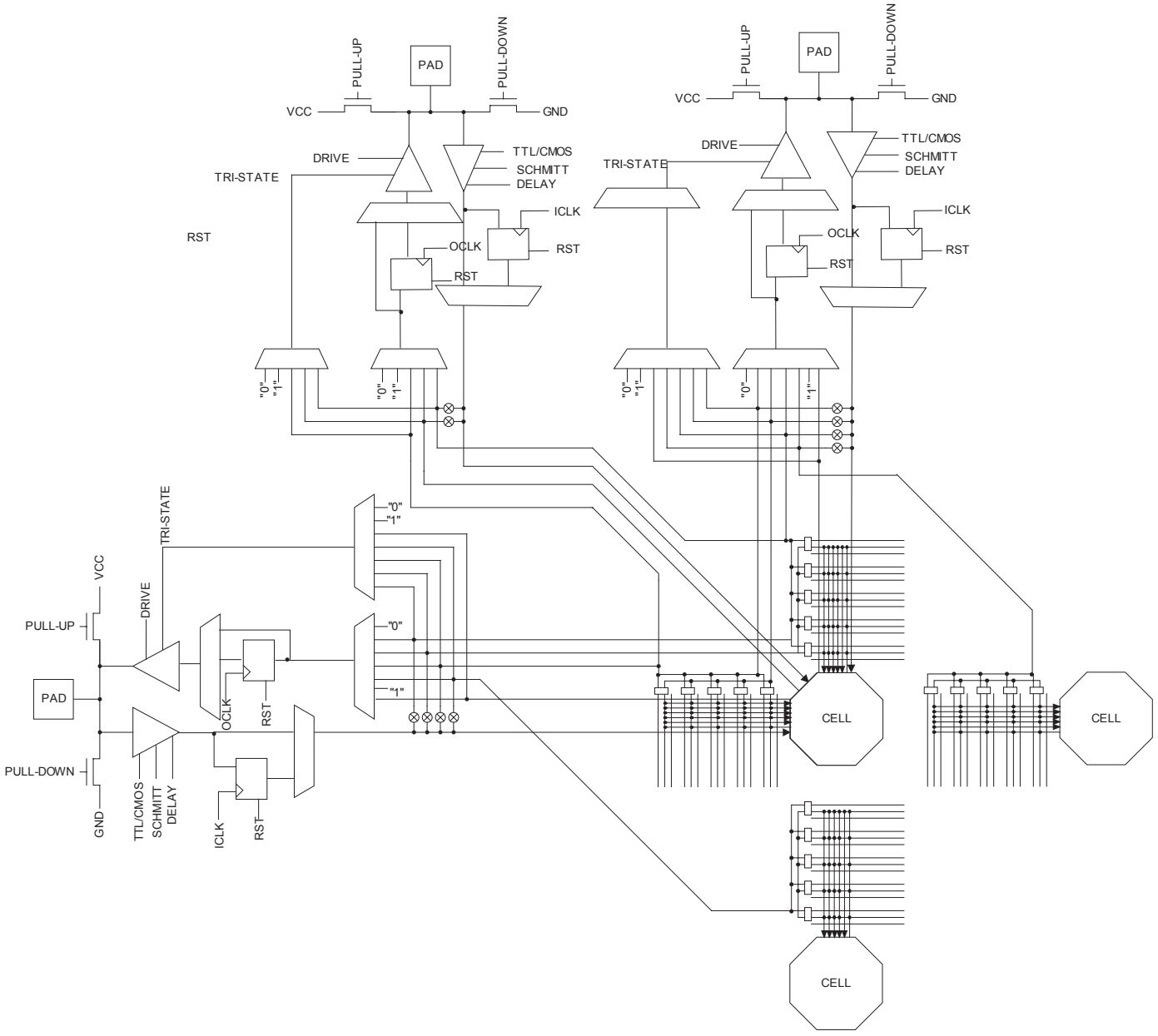


a. Primary I/0



b. Secondary I/O

Figure 14. Northwest Corner I/O (Similar NE/SE/SW Corners)



Electrical Characteristics

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Junction Temperature	+150°C
Voltage on Any Input Pin with Respect to Ground (1)	-0.5V to 5.5V DC (KEL version)
	-0.5V to 7.0V DC (KFL version)
Voltage on Any Output Pin with Respect to Ground	-0.5V to 5.5V DC
Supply Voltage (V_{CC})	-0.5V to 5.5V
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	4000V

*Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

1. For DC Input Voltage (V_I) Minimum voltage of -0.5V DC, which may undershoot to -2.0V for pulses of less than 20 ns.

DC and AC Operating Range

Operating Temperature		-55°C to +125°C
V_{CC} Power Supply		3.3V ± 0.3V
Input Voltage Level (CMOS)	High (V_{IHC})	70% V_{CC} to V_{CC} + 0.3V DC (KEL version) 70% V_{CC} to 5.5V DC (KFL version)
	Low (V_{ILC})	-0.3V to 30% V_{CC} DC

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level Input Voltage	CMOS	70% V_{CC}			V
		TTL	2.0			V
V_{IL}	Low-level Input Voltage	CMOS	-0.3		30% V_{CC}	V
		TTL	-0.3		0.8	V
V_{OH}	High-level Output Voltage	I_{OH} = -4 mA V_{CC} = 3.3V	2.4			V
		I_{OH} = -12 mA V_{CC} = 3.3V	2.4			V
		I_{OH} = -16 mA V_{CC} = 3.3V	2.4			V
V_{OL}	Low-level Output Voltage	I_{OL} = +4 mA V_{CC} = 3.3V			0.4	V
		I_{OL} = +12 mA V_{CC} = 3.3V			0.4	V
		I_{OL} = +16 mA V_{CC} = 3.3V			0.4	V
I_{IH}	High-level Input Current	V_{IN} = V_{CC} max	-5		5	µA
		With pull-down, V_{IN} = V_{CC}	20	75	300	µA
I_{IL}	Low-level Input Current	V_{IN} = V_{SS}	-5		5	µA
		With pull-up, V_{IN} = V_{SS}	-300.0	-50	-20	µA
I_{OZH}	High-level Tri-state Output Leakage Current	Without pull-down, V_{OUT} = V_{CC} max	-5		5	µA
		With pull-down, V_{OUT} = V_{CC} max	20		300	µA
I_{OZL}	Low-level Tri-state Output Leakage Current	Without pull-up, V_{OUT} = V_{SS}	-5			mA
		With pull-up, V_{OUT} = V_{SS} for CON	-500	-150.0	-110	µA
I_{CC}	Standby Current Consumption	Standby, unprogrammed		1	5	mA
C_{IN}	Input Capacitance[1]	All pins			10	pF

Note: 1. Parameter based on characterization and simulation; it is not tested in production.

Power-On Supply Requirements

Atmel FPGAs require a minimum rated power supply current capacity to ensure proper initialization, and the power supply ramp-up time does not affect the current required. A fast ramp-up time requires more current than a slow ramp-up time.

Table 3. Power-on Supply Requirements

Description	Maximum Current[1][2]
Maximum Current Supply	1.2 A

Note: 1. Devices are guaranteed to initialize properly at 50% of the minimum current listed above. A larger capacity power supply may result in a larger initiallization current.

2. Ramp-up time is measured from 0V DC to 3.6V DC. Peak current required lasts less than 2 ms, and occurs near the internal power on reset threshold voltage.

AC Timing Characteristics

Delays are based on fixed loads which are described in the notes.
Maximum timing based on worst case: V_{cc} = 3.0V, temperature = 125°C.
Minimum timing based on best case: V_{cc} = 3.6V, temperature = -55°C.
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	Value	Unit	Notes
Core					
2-input gate	t_{PD} (max)	x/y -> x/y	2.9	ns	1 unit load
3-input gate	t_{PD} (max)	x/y/z -> x/y	3.1	ns	1 unit load
3-input gate	t_{PD} (max)	x/y/w -> x/y	3.5	ns	1 unit load
4-input gate	t_{PD} (max)	x/y/w/z -> x/y	3.5	ns	1 unit load
Fast carry	t_{PD} (max)	y -> y	2.8	ns	1 unit load
Fast carry	t_{PD} (max)	x -> y	2.6	ns	1 unit load
Fast crry	t_{PD} (max)	y -> x	2.8	ns	1 unit load
Fast carry	t_{PD} (max)	x -> x	2.9	ns	1 unit load
Fast carry	t_{PD} (max)	w -> y	3.5	ns	1 unit load
Fast carry	t_{PD} (max)	w -> x	3.5	ns	1 unit load
Fast carry	t_{PD} (max)	z -> y	3.1	ns	1 unit load
Fast carry	t_{PD} (max)	z -> x	3.0	ns	1 unit load
DFF	t_{PD} (max)	Clk -> x/y	4.3	ns	1 unit load
DFF	t_{PD} (max)	R -> x/y	4.1	ns	1 unit load
DFF	t_{PD} (max)	S -> x/y	2.8	ns	1 unit load
DFF	t_{PD} (max)	q -> w	4.3	ns	
Incremental -> L	t_{PD} (max)	x/y -> L	2.5	ns	1 unit load
Local output enable	t_{PZX} (max)	oe -> L	2.9	ns	1 unit load
Local output enable	t_{PXZ} (max)	oe -> L	0.9	ns	

AC Timing Characteristics

All input I/O characteristics measured from V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}.
All output I/O characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	Value	Unit	Notes
Repeaters					
Repeater	t_{PD} (max)	L -> E	1.3	ns	1 unit load
Repeater	t_{PD} (max)	E -> E	1.3	ns	1 unit load
Repeater	t_{PD} (max)	L -> L	1.3	ns	1 unit load
Repeater	t_{PD} (max)	E -> L	1.3	ns	1 unit load
Repeater	t_{PD} (max)	E -> IO	0.7	ns	1 unit load
Repeater	t_{PD} (max)	L -> IO	0.7	ns	1 unit load

Cell Function	Parameter	Path	Value	Unit	Notes
I/O					
Input	t_{PD} (max)	pad -> x/y	5.4	ns	no extra delay
Input	t_{PD} (max)	pad -> x/y	7.6	ns	1 extra delay
Input	t_{PD} (max)	pad -> x/y	11.4	ns	2 extra delays
Input	t_{PD} (max)	pad -> x/y	14.9	ns	3 extra delays
Output, slow	t_{PD} (max)	x/y/E/L -> pad	16.0	ns	50 pf load
Output, medium	t_{PD} (max)	x/y/E/L -> pad	14.8	ns	50 pf load
Output, fast	t_{PD} (max)	x/y/E/L -> pad	11.2	ns	50 pf load
Output, slow	t_{PZX} (max)	oe -> pad	16.4	ns	50 pf load
Output, slow	t_{PXZ} (max)	oe -> pad	5.1	ns	50 pf load
Output, medium	t_{PZX} (max)	oe -> pad	14.1	ns	50 pf load
Output, medium	t_{PXZ} (max)	oe -> pad	9.1	ns	50 pf load
Output, fast	t_{PZX} (max)	oe -> pad	11.4	ns	50 pf load
Output, fast	t_{PXZ} (max)	oe -> pad	9.5	ns	50 pf load

AC Timing Characteristics

Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{CC}. Maximum timings for clock input buffers and internal drivers are measured for rising edge delays only.

Cell Function	Parameter	Path	Value	Unit	Notes
Global Clocks and Set/Reset					
GCK Input buffer	t_{PD} (max)	pad -> clock	3.3	ns	rising edge clock
FCK Input buffer	t_{PD} (max)	pad -> clock	1.9	ns	rising edge clock
Clock column driver	t_{PD} (max)	clock -> colclk	1.7	ns	rising edge clock
Clock sector driver	t_{PD} (max)	colclk -> secclk	0.8	ns	rising edge clock
GSRN Input buffer	t_{PD} (max)	colclk -> secclk	10.3	ns	
Global clock to output	t_{PD} (max)	clock pad -> out	21.3	ns	rising edge clock fully loaded clock tree rising edge DFF 20 mA output buffer 50 pf pin load
Fast clock to output	t_{PD} (max)	clock pad -> out	19.9	ns	rising edge clock fully loaded clock tree rising edge DFF 20 mA output buffer 50 pf pin load

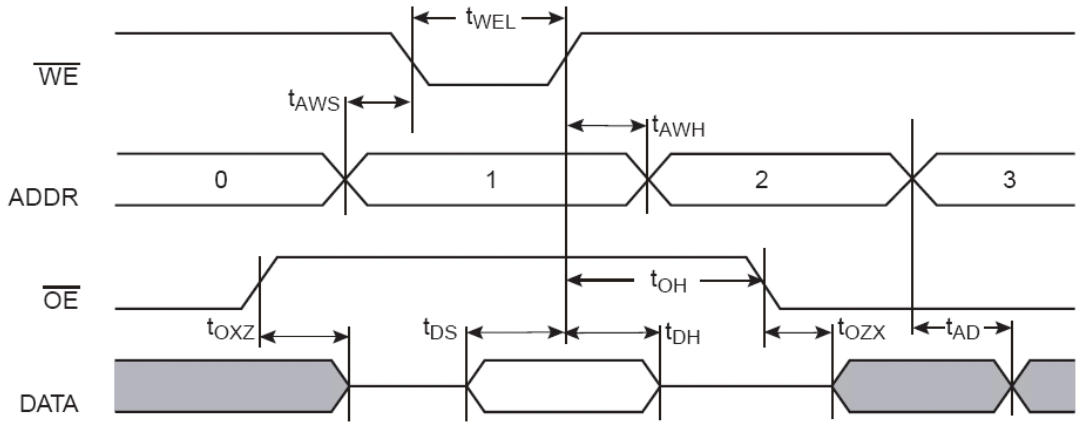
Notes:
1. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. Buffer delay is to a pad voltage of 1.5V with one output switching.
3. Parameter based on characterization and simulation; not tested in production.
4. Exact power calculation is available in Atmel FPGA Designer software.

AC Timing Characteristics

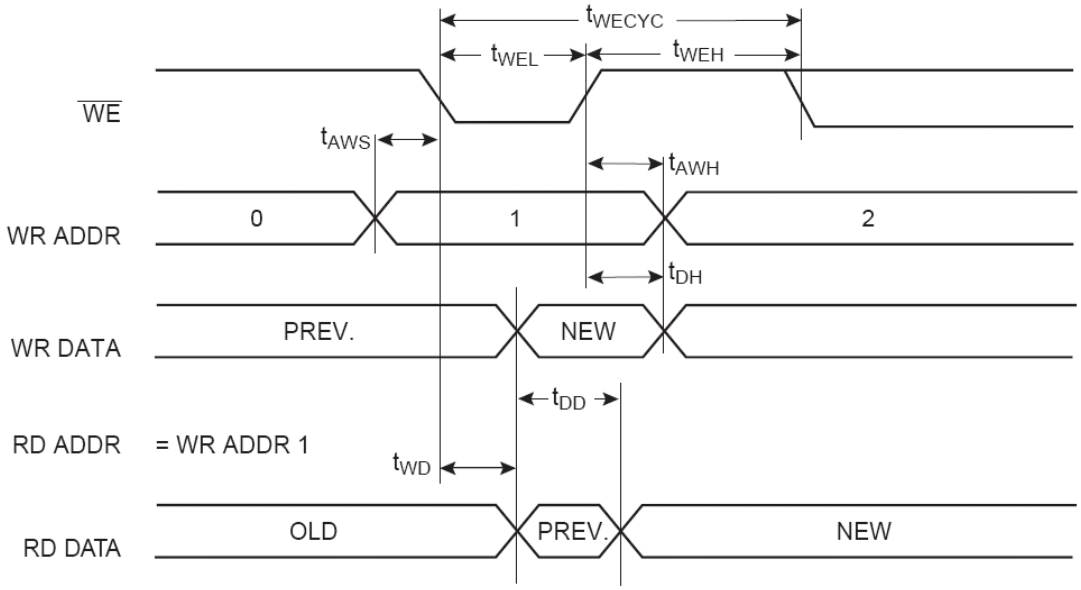
Cell Function	Parameter	Path	Value	Unit	Notes
Asynchronous RAM					
Write	t_{WECYC} (min)	cycle time	28	ns	
Write	t_{WEL} (min)	we	6.5	ns	pulse width low
Write	t_{WEH} (min)	we	6.5	ns	pulse width high
Write	t_{setup} (min)	wr addr setup -> we	7.0	ns	
Write	t_{hold} (min)	wr addr hold -> we	0.0	ns	
Write	t_{setup} (min)	din setup -> we	6.5	ns	
Write	t_{hold} (min)	din hold -> we	0.0	ns	
Write	t_{hold} (min)	oe hold -> we	0.0	ns	
Write/Read	t_{PD} (max)	din -> dout	14.1	ns	rd addr = wr addr
Read	t_{PD} (max)	rd addr -> dout	13.1	ns	
Read	t_{PZX} (max)	oe -> dout	4.5	ns	
Read	t_{PXZ} (max)	oe -> dout	4.5	ns	
Synchronous RAM					
Write	t_{CYC} (min)	cycle time	28	ns	
Write	t_{CLKL} (min)	clk	6.5	ns	pulse width low
Write	t_{CLKH} (min)	clk	6.5	ns	pulse width high
Write	t_{setup} (min)	we setup -> clk	5.0	ns	
Write	t_{hold} (min)	we hold -> clk	0.0	ns	
Write	t_{setup} (min)	wr addr setup -> clk	6.5	ns	
Write	t_{hold} (min)	wr addr hold -> clk	0.0	ns	
Write	t_{setup} (min)	wr data setup -> clk	5.1	ns	
Write	t_{hold} (min)	wr data hold -> clk	0.0	ns	
Write/Read	t_{PD} (max)	din -> dout	14.1	ns	rd addr = wr addr
Write/Read	t_{PD} (max)	clk -> dout	7.9	ns	rd addr = wr addr
Read	t_{PD} (max)	rd addr -> dout	13.1	ns	
Read	t_{PZX} (max)	oe -> dout	4.5	ns	
Read	t_{PXZ} (max)	oe -> dout	4.5	ns	

FreeRAM Asynchronous Timing Characteristics

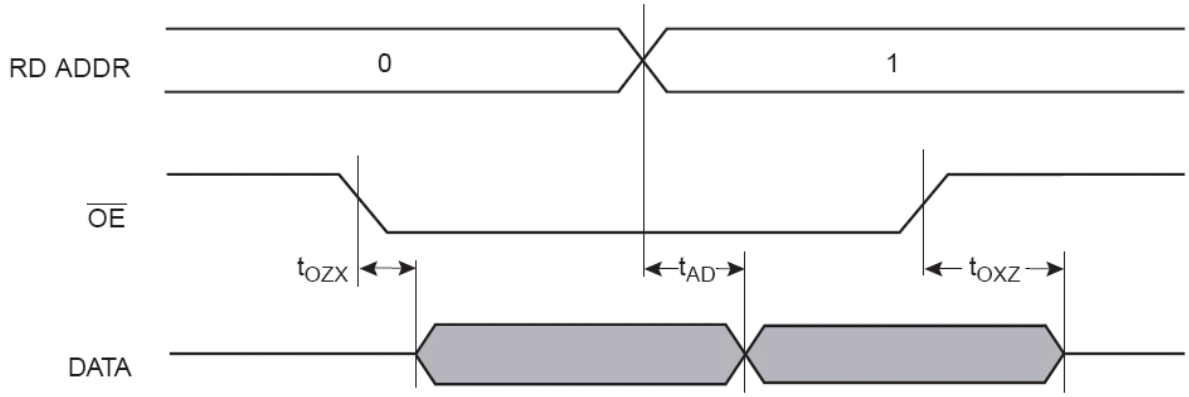
Single Port Write/Read



Dual Port Write with Read

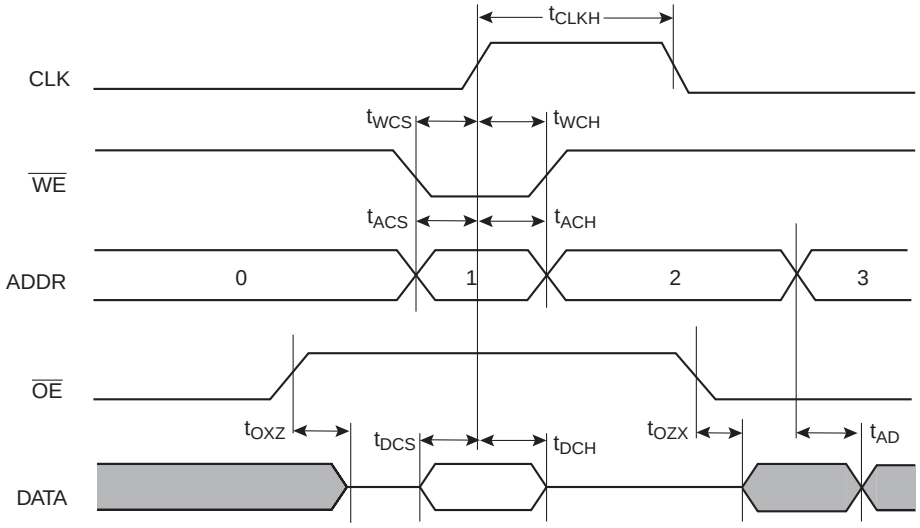


Dual Port Read

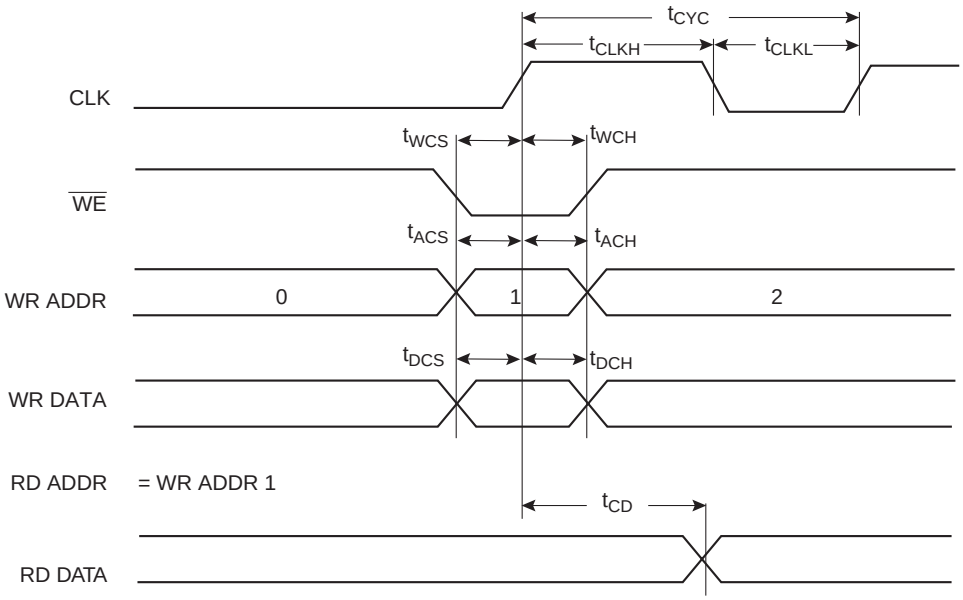


FreeRAM Synchronous Timing Characteristics

Single Port Write/Read



Dual Port Write with Read



Dual Port Read

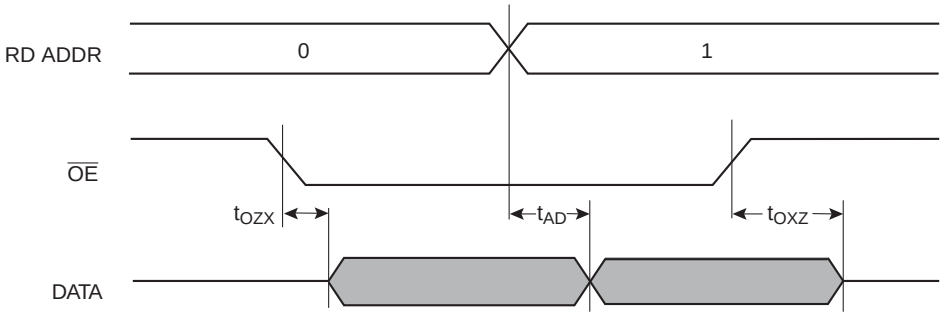


Table 4. MQFP F-160

Pin Number	Signal
1	VCC
2	I/O384_GCK8_A15
3	I/O383_A14
4	I/O382
5	I/O381
6	I/O372_A13
7	I/O371_A12
8	I/O370
9	I/O369
10	GND
11	I/O360
12	I/O359
13	I/O348_A11
14	I/O347_A10
15	I/O344
16	I/O343
17	I/O338_A9
18	I/O337_A8
19	VCC
20	GND
21	I/O336_A7
22	I/O335_A6
23	I/O330
24	I/O329
25	I/O328
26	I/O326_A5
27	I/O325_A4
28	I/O314
29	I/O313
30	GND
31	I/O304
32	I/O303
33	I/O298_A3
34	I/O297_CS1_A2
35	I/O292
36	I/O291
37	I/O290_GCK7_A1
38	I/O289_A0
39	GND
40	TESTCLOCK
41	VCC
42	CCLK
43	I/O288_GCK6
44	I/O287_D0
45	I/O286
46	I/O285
47	I/O278
48	I/O277_D1
49	I/O274
50	I/O273
51	GND
52	I/O262_FCK4
53	I/O261
54	I/O260
55	I/O259_D2
56	I/O246
57	I/O245
58	I/O242_CHECK
59	I/O241_D3
60	GND
61	VCC
62	I/O240
63	I/O239_D4
64	I/O236
65	I/O235
66	I/O222_CS0
67	I/O221_D5
68	I/O220
69	I/O219_FCK3
70	GND
71	I/O208
72	I/O207
73	I/O206
74	I/O205_D6
75	I/O196
76	I/O195
77	I/O194_GCK5
78	I/O193_D7
79	RESETN
80	VCC
81	CON
82	GND
83	I/O192_GCK4
84	I/O191_D8
85	I/O190
86	I/O189
87	I/O184_D9
88	I/O183_D10
89	I/O180
90	I/O179
91	GND
92	I/O168
93	I/O167
94	I/O166_D11
95	I/O165_D12
96	I/O152
97	I/O151
98	I/O146_D13
99	I/O145_D14
100	GND
101	VCC

Pin Number	Signal
102	I/O144_INIT
103	I/O143_D15
104	I/O138
105	I/O137
106	I/O124
107	I/O123
108	I/O122
109	I/O121
110	GND
111	I/O110
112	I/O109
113	I/O102_LDC
114	I/O101
115	I/O100
116	I/O99
117	I/O98_HDC
118	I/O97_GCK3
119	M2
120	VCC
121	M0
122	GND
123	M1
124	I/O96_GCK2
125	I/O95_OTS
126	I/O94
127	I/O93
128	I/O90
129	I/O89
130	I/O84
131	I/O83
132	GND
133	I/O72_FCK2
134	I/O71
135	I/O70

Pin Number	Signal
136	I/O69
137	I/O54
138	I/O53
139	I/O50
140	I/O49
141	VCC
142	GND
143	I/O48_A23
144	I/O47_A22
145	I/O44
146	I/O43
147	I/O28_A21
148	I/O27_A20
149	I/O26
150	I/O25_FCK1
151	GND
152	I/O16
153	I/O15
154	I/O6_A19
155	I/O5_A18
156	I/O4
157	I/O3
158	I/O2_A17
159	I/O1_GCLK1_A16
160	GND

Table 5. MQFP - F256

Pin Number	Signal
1	IO384_GCK8_A15
2	IO383_A14
3	IO382
4	IO381
5	IO378
6	IO377
7	GND
8	VCC
9	IO375
10	IO374
11	IO372_A13
12	IO371_A12
13	IO370
14	IO369
15	IO366
16	IO365
17	IO362
18	IO360
19	IO359
20	IO358
21	IO356
22	IO355
23	IO353
24	IO352
25	IO349
26	IO348_A11
27	IO347_A10
28	IO346
29	IO344
30	IO343
31	IO338_A9
32	IO337_A8
33	IO336_A7
34	IO335_A6
35	IO334
36	IO330
37	IO329
38	IO328
39	IO326_A5
40	IO325_A4
41	IO324
42	IO323
43	IO321
44	IO320
45	IO318
46	IO317
47	IO314
48	IO313
49	IO312
50	IO311
51	IO308
52	IO307
53	IO304
54	IO303
55	IO301
56	IO298_A3
57	GND
58	VCC
59	IO297_CS1_A2
60	IO291
61	IO292
62	IO290_GCK7_A1
63	IO289_A0
64	TESTCLOCK
65	CCLK
66	IO288_GCK6
67	IO287_D0
68	IO286
69	IO285
70	IO282
71	GND
72	VCC
73	IO278
74	IO277_D1
75	IO276
76	IO274
77	IO273
78	IO272
79	IO270
80	IO269
81	IO267
82	IO266
83	IO262_FCK4
84	IO261
85	IO260
86	IO259_D2
87	IO258
88	IO257
89	IO254
90	IO253
91	IO252
92	IO251
93	IO248
94	IO246
95	IO245
96	IO242_CHECK
97	IO241_D3
98	IO240
99	IO239_D4
100	IO236
101	IO235

Pin Number	Signal
102	IO234
103	IO232
104	IO230
105	IO228
106	IO227
107	IO225
108	IO224
109	IO222_CS0
110	IO221_D5
111	IO220
112	IO219_FCK3
113	IO216
114	IO215
115	IO212
116	IO208
117	IO207
118	IO206
119	IO205_D6
120	IO204
121	GND
122	VCC
123	IO203
124	IO196
125	IO195
126	IO194_GCK5
127	IO193_D7
128	RESETN
129	CON
130	IO192_GCK4
131	IO191_D8
132	IO190
133	IO189
134	IO186
135	GND

Pin Number	Signal
136	VCC
137	IO184_D9
138	IO183_D10
139	IO181
140	IO180
141	IO179
142	IO177
143	IO174
144	IO173
145	IO171
146	IO168
147	IO167
148	IO166_D11
149	IO165_D12
150	IO163
151	IO162
152	IO161
153	IO158
154	IO157
155	IO156
156	IO152
157	IO151
158	IO150
159	IO149
160	IO146_D13
161	IO145_D14
162	IO144_INIT
163	IO143_D15
164	IO141
165	IO138
166	IO137
167	IO136
168	IO134
169	IO132

Pin Number	Signal
170	IO131
171	IO129
172	IO128
173	IO124
174	IO123
175	IO122
176	IO121
177	IO120
178	IO119
179	IO116
180	IO115
181	IO113
182	IO110
183	IO109
184	IO101
185	GND
186	VCC
187	IO102_LDC
188	IO99
189	IO100
190	IO98_HDC
191	IO97_GCK3
192	M2
193	M0
194	M1
195	IO96_GCK2
196	IO95_OTS
197	IO94
198	IO93
199	GND
200	VCC
201	IO90
202	IO89
203	IO86

Pin Number	Signal
204	IO85
205	IO84
206	IO83
207	IO80
208	IO79
209	IO77
210	IO76
211	IO72_FCK2
212	IO71
213	IO70
214	IO69
215	IO67
216	IO66
217	IO63
218	IO62
219	IO60
220	IO59
221	IO57
222	IO56
223	IO54
224	IO53
225	IO50
226	IO49
227	IO48_A23
228	IO47_A22
229	IO44
230	IO43
231	IO41
232	IO39
233	IO36
234	IO35
235	IO34
236	IO33
237	IO30

Pin Number	Signal
238	IO29
239	IO28_A21
240	IO27_A20
241	IO26
242	IO25_FCK1
243	IO21
244	IO20
245	IO18
246	IO16
247	IO15
248	IO13
249	GND
250	VCC
251	IO6_A19
252	IO5_A18
253	IO4
254	IO3
255	IO2_A17
256	IO1_GCLK1_A16

Part/Package Availability and User I/O Counts (Including Dual-function Pins)

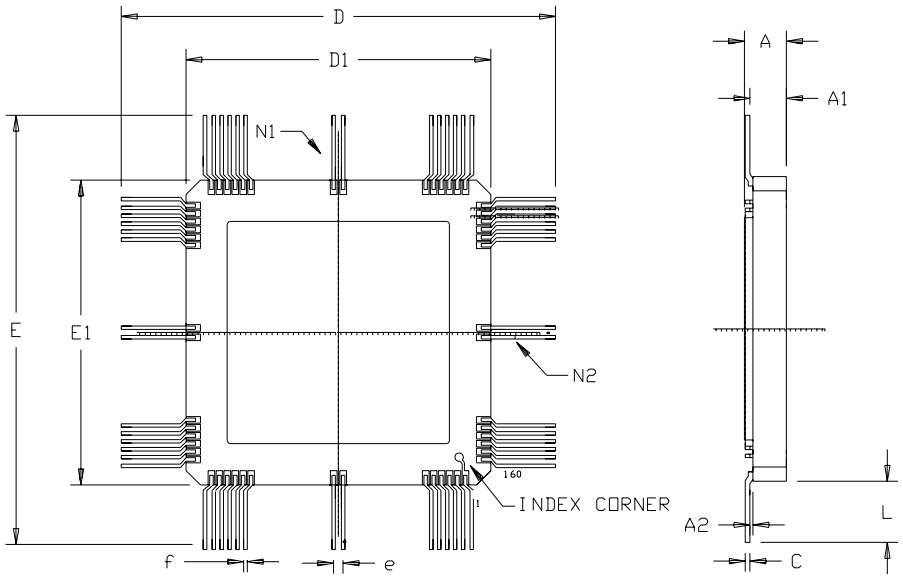
Package	AT40KEL040
MQFPF 160	129
MQFPF 256	233

Ordering Information

Part Number	Package	Version	Temperature Range	Quality Flow
AT40KEL040KW1-E	MQFPF160	3.3V	25°C	Engineering Samples
5962-0325001QXC	MQFPF160	3.3V	-55° to +125°C	QML Q
5962-0325001VXC	MQFPF160	3.3V	-55° to +125°C	QML V
930400801	MQFPF160	3.3V	-55° to +125°C	ESCC
AT40KEL040KZ1-E	MQFPF256	3.3V	25°C	Engineering Samples
5962-0325001QYC	MQFPF256	3.3V	-55° to +125°C	QML Q
5962-0325001VYC	MQFPF256	3.3V	-55° to +125°C	QML V
930400802	MQFPF256	3.3V	-55° to +125°C	ESCC
AT40KFL040KW1-E	MQFPF160	3.3V, 5V Tolerant	25°C	Engineering Samples
5962-0325002QXC	MQFPF160	3.3V, 5V Tolerant	-55° to +125°C	QML Q
5962-0325002VXC	MQFPF160	3.3V, 5V Tolerant	-55° to +125°C	QML V
AT40KFL040KW1-SCC	MQFPF160	3.3V, 5V Tolerant	-55° to +125°C	ESCC
AT40KFL040KZ1-E	MQFPF256	3.3V, 5V Tolerant	25°C	Engineering Samples
5962-0325002QYC	MQFPF256	3.3V, 5V Tolerant	-55° to +125°C	QML Q
5962-0325002VYC	MQFPF256	3.3V, 5V Tolerant	-55° to +125°C	QML V
AT40KFL040KZ1-SCC	MQFPF256	3.3V, 5V Tolerant	-55° to +125°C	ESCC

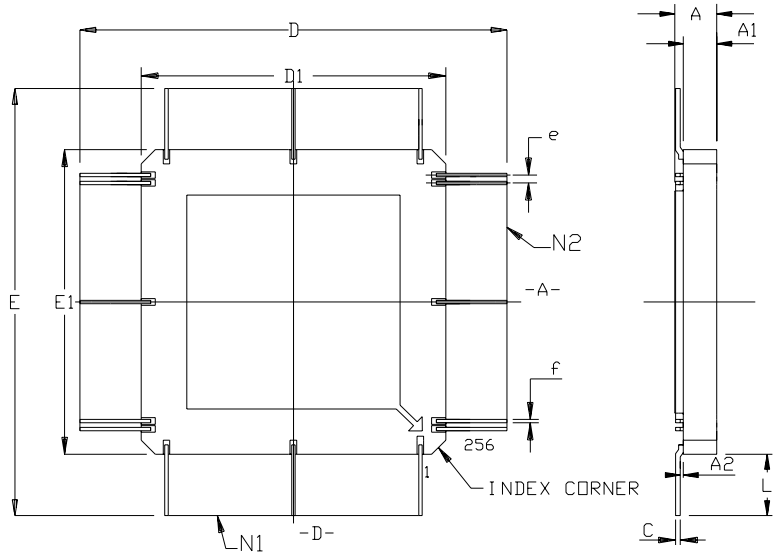
Package Drawing

Multilayer Quad Flat Pack (MQFP) 160-pin - Front View



	mm		mils	
	Min	Max	Min	Max
A	1.96	2.66	.077	.105
C	0.10	0.20	.004	.008
D	37.90	39.30	1.492	1.548
D1	26.90	27.50	1.059	1.083
E	37.90	39.30	1.492	1.548
E1	26.90	27.50	1.059	1.083
e	0.650 BSC		.0256 BSC	
f	0.25	0.35	.010	.014
A1	1.70	2.10	.067	.083
A2	0.10	0.30	.004	.012
L	5.50	5.90	.216	.232
N1	40		40	
N2	40		40	

Multilayer Quad Flat Pack (MQFP) 256-pin - Front View



	mm		mils	
	Min	Max	Min	Max
A	2.41	3.18	.095	.125
C	0.10	0.20	.004	.008
D	53.23	55.74	2.095	2.195
D1	36.83	37.34	1.450	1.470
E	53.23	55.74	2.095	2.195
E1	36.83	37.34	1.450	1.470
e	0.508 BSC		.020 BSC	
f	0.15	0.25	.006	.010
A1	2.06	2.56	.081	.101
A2	0.05	0.36	.002	.014
L	8.20	9.20	.323	.362
N1	64		64	
N2	64		64	

Datasheet Change Log

Changes from 4155B - 06/03 to 4155C 04/04

1. Addition of MQFP F256 package information
2. Pad/ Pin assignment updated. Table 4 on page 31.
3. Ordering information updated
4. Reference to design tools

Changes from 4155C - 06/03 to 4155D 04/04

1. Update of radiation hardness performance, page 1.

Changes from 4155D 04/04 - to 4155E 06/04

1. Updated FreeRAM timing characteristics, Section “FreeRAM Asynchronous Timing Characteristics”, page 29.

Changes from 4155E 06/04 to 4155F 06/04

1. Minor changes throughout the document.

Changes from 4155F 06/04 to 4155G 05/05

1. Minor changes.

Changes from 4155G 05/05 to 4155H 02/06

1. Added MQFP256 package.

Changes from 4155H 02/06 to 4155I 06/06

1. Adding AT40KFL040 5V tolerant version.
2. Corrections on matrix decription.

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